

ABSTRACT

The present invention relates to the reduction of critical dimensions and the reduction of feature sizes in manufacturing integrated circuits. Specifically, the method controls photoresist flow rates to develop critical dimensions beyond the resolution limits of the photoresist material used, and the limits of lithographic tool sets. The post exposure and developed resist pattern is exposed to a solvent prior to a bake or reflow process. Exposure to the solvent lowers the molecular weight of the resist material, modifying the resist material's reflow rate. The post-exposure resist is then easier to control during a subsequent reflow process to reduce the hole or line size of the patterned resist.